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EXAMINER	
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ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/750,954	AIGO, TAKAO	
	Examiner	Art Unit	
	MICHAEL C. KROFCHECK	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9 and 10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9 and 10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the RCE filed on 3/20/2008.

2. Claims 1-7 and 9-10 have been amended.

3. Claims 8 and 11-16 have been cancelled.

4. The objections/rejections from the prior correspondence not restated herein have been withdrawn.

Specification

5. The disclosure is objected to because of the following informalities:

a. As laid out below, page 1, lines 10-27 and page 6 lines 2-9 indicate that a multitask process is executed based on an I/O process (read/write process), the multitask process is a process that contains a plurality of tasks that are independent and occur simultaneously. Each task also executes on I/O process. These two statements contradict each other since each task cannot be one I/O process and makeup part of a multitask which also is the same I/O process.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claims 1-7 and 9-10 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

8. Independent claims 1-7 and 9-10 indicate that a multitask is generated for processing a single I/O request, a multitask being defined by the claim as, "first tasks with a first priority and second tasks with a second priority that is lower than the first priority." In other words, as a result on a single I/O request (read/write request, specification page 1, lines 12-13), numerous tasks are generated to accomplish the single read/write request. This concept of using numerous tasks to accomplish a single task is not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

9. Claims 1-7 and 9-10 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

10. Independent claims 1, 3, and 6, recite “a control element…generat[ing] a multitask for processing a single I/O process.” However, the examiner is unable to find support for a control element generating a multitask from a single I/O process in the

applicant's specification. Page 6, lines 4-6 indicate executing a multitask process based on an I/O process, and figure 3 shows generating tasks, but do not disclose generating a multitask for processing a single I/O process.

11. Additionally claims 1, 3, and 6, recite a second element constructed and arranged so that when the single I/O request is input to the disk array control apparatus, the second element executes the first tasks..." The applicant's specification does not support for executing first and second tasks when the single I/O request is input to the disk array control apparatus.

12. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

13. Claims 1-7 and 9-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

14. Regarding independent claims 1, 3, and 6, the phrase "...generates a multitask for processing a single I/O request, the multitask including first tasks with a first priority and second tasks with a second priority..." renders the claim indefinite. The claims define that a multitask consists of numerous other tasks and a multitask corresponds to one I/O request. However, the applicant's specification indicates that one task corresponds to one I/O process and numerous tasks can execute concurrently as numerous I/O processes executing concurrently in page 1, lines 22-23 of the applicant's specification. These two accounts are contradictory and render the metes and bounds of the claims unclear. Is the applicant's intent to claim that a task generated to process

a single I/O request is multitasked with other tasks that process other single I/O requests, where the multitasked tasks include the respective priorities? It is the examiner interpretation based on the applicant's specification and description that the control element generates a multitasked task for processing a single I/O request, the multitasking including first tasks with a first priority and second tasks with a second priority that is lower than the first priority.

Furthermore the term, "multitask" is a verb, yet the applicants are using it as a noun which adds to the possible confusion of the claimed bounds.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

17. Claim 1-7, 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over O'Neil et al. (6085287), Johnson et al. (63082485), and Ryan (5367656).

18. With respect to claim 1, 3, and 6, O'Neil teaches of a disk array control apparatus/method comprising: a first element constructed and arranged so that the first element calculates a cache hit ratio at a disk cache memory (fig. 2; item 26; column 3, lines 55-57).

O'Neil fails to specifically teach of a control element constructed and arranged so that the control element generates a multitask for processing a single I/O request, the multitask including first tasks with a first priority and second tasks with a second priority that is lower than the first priority, wherein an upper limit of a number of the first tasks is a first number; a second element constructed and arranged so that when new tasks are input to the disk array control apparatus the second element executes the new tasks as a first priority unless a number of the new tasks and tasks in execution exceeds a first number, and executes the new tasks as a second priority when the number of the new tasks and tasks in execution as the first priority exceeds the first number, wherein the first priority is higher than the second priority.

However, Johnson teaches of a control element constructed and arranged so that the control element generates a multitask for processing a single I/O request (column 2, lines 40-48),

the multitasking including first tasks with a first priority and second tasks with a second priority that is lower than the first priority, wherein an upper limit of a number of the first tasks is a first number (fig. 8, column 9, lines 20-62);

a second element constructed and arranged so that when the single I/O request is input to the disk array control apparatus the second element executes the first tasks until the number of the first tasks reaches the first number (fig. 8; column 9, lines 20-62; where the number of tasks executed are not to exceed a minimum number), and

executes the second tasks and the first tasks when the number of the first tasks reaches the first number, (fig. 8; column 9, lines 20-62; where if the minimum is exceeded a task is put to sleep (2^{nd} priority). A sleeping task is of a lower priority than an active task),

Ryan teaches of except that the second element executes only the first tasks when the calculated cache hit ratio is above a prescribed value even if the number of first tasks reaches the first number (fig. 1, 5; column 3, line 51-column 4, line 14; column 8, lines 63-column 9, line 7; when the hit ratio is below the threshold, the miss prediction is enabled, so that miss prediction occurs and regular cache accessing occurs. The regular cache accessing by the main processor, i.e. the main processor requesting operands/data from the memory, etc, are high priority tasks since they are required for processor to carry out the program. The miss prediction is a low priority task because it just enhances the performance of the cache memory, it is not required for the main processor carry out the program. When the hit ratio is above the threshold, the miss prediction is disabled, and so only the tasks from the processor are carried out).

It would have been obvious to one of ordinary skill in the art having the teachings of O'Neil and Johnson at the time of the invention to include the task management of

Johnson in O'Neil. Their motivation would have been to limit spikes in workload, and thus achieve better performance (Johnson, column 2, lines 34-39).

It would have been obvious to one of ordinary skill in the art having the teachings of O'Neil, Johnson, and Ryan at the time of the invention to include the cache predictive prefetching system of Ryan in the cache memory system of the combination of O'Neil, and Johnson. Their motivation would have been to lower the cache miss ratio (Ryan, column 2, lines 40-42).

19. With respect to claims 2 and 7, Ryan teaches of wherein a number tasks in the multitask decreases when the calculated cache hit ratio is above the prescribed value and increases when the calculated cache hit ratio is below the prescribed value (fig. 1, 5; column 8, lines 63-column 9, line 7).

20. With respect to claim 4, O'Neil teaches of a host I/O reception unit arranged so that the host I/O reception unit receives as an input the single I/O process request from a host computer, the I/O reception unit generating as an output the single I/O process request (fig. 2; item 22, column 3, lines 54-65) and a disk cache memory (fig. 2; item 18),

wherein the first element includes a cache hit determination unit constructed and arranged to determine whether or not the single I/O process request is causing a cache hit at the cache memory (fig. 2; item 26; column 3, lines 55-57);

a cache hit ratio monitor unit constructed and arranged to calculate and output the cache hit ratio within some period of time by using a determination result of the cache hit determination unit (fig. 2; item 26; column 3, lines 55-57);

Ryan teaches of wherein the first element includes a cache hit determination unit constructed and arranged to determine whether or not the single I/O process request is causing a cache hit at the cache memory (fig. 2; column 4, lines 7-14);

a cache hit ratio monitor unit constructed and arranged to calculate and output the cache hit ratio within some period of time by using a determination result of the cache hit determination unit (fig. 1, 5; column 2, lines 58-63; as it must be known if the request is a cache hit or miss to calculate the ratio, the hit ratio must be calculated based on wither the requests were hits or misses in the cache memory).

21. With respect to claim 9, Ryan teaches of a inputting the single I/O request from a host computer (fig. 2; column 4, lines 7-10);

determining whether the single I/O request is causing a cache hit at a cache memory (fig. 2; column 4, lines 7-14);

calculating the cache hit ratio within some period of time based on results of the determining step (fig. 1, 5; column 2, lines 58-63; as it must be known if the request is a cache hit or miss to calculate the ratio of such, the hit ratio must be calculated based on wither the requests were hits or misses in the cache memory).

O'Neil teaches of calculating a cache hit ratio within some period of time at a disk cache memory (fig. 2; item 26; column 3, lines 55-57).

22. Claims 5, 10 rejected under 35 U.S.C. 103(a) as being unpatentable over Ryan, O'Neil, Johnson as applied to claims 4, 9, respectively, and further in view of Horii et al., JP 08-077025 A.

23. With respect to claims 5, 10, O'Neil fails to specifically teach of a task priority change unit constructed and arranged to dynamically change the one of the second tasks to one of the first tasks after starting execution of the one of the second tasks, the task priority change unit changing the changed task back to one of the second tasks at execution termination time.

However, Horii teaches of a task priority change unit constructed and arranged to dynamically change the one of the second tasks to one of the first tasks after starting execution of the one of the second tasks, the task priority change unit changing the changed task back to one of the second tasks at execution termination time (paragraph 0009).

It would have been obvious to one of ordinary skill in the art having the teachings of Ryan, O'Neil, Johnson, and Horii at the time of the invention to modify the priority of the tasks while they are being executed as taught in Horii. Their motivation would have been to avoid the inversion phenomenon of priority, where a low priority task is executed before a high priority task (Horii, paragraph 0005).

Response to Arguments

24. Applicant's arguments filed 3/20/2008 have been fully considered but they are not persuasive.

25. Applicant argues with respect to the independent claims that Ryan's disclosed operations, miss prediction and cache accessing are separate operations an not part of the applicant's multitask. The examiner disagrees. The applicant never indicates what

types of tasks the claimed tasks are (similar or dissimilar) and also does not indicate that the tasks must be the same "type" of task. Ryan's tasks (cache accessing and cache miss prediction) all perform I/O operations on the cache memory. As such, the combination including Ryan above reads on the applicant's claims.

Conclusion

26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Krofcheck whose telephone number is 571-272-8193. The examiner can normally be reached on Monday - Friday.

27. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

28. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/MICHAEL C KROFCHECK/
Examiner, Art Unit 2186

/Matt Kim/
Supervisory Patent Examiner, Art Unit 2186

Michael Krofcheck